

Claims

- [c1] A semiconductor structure comprising:
a doped semiconductor substrate;
a monolayer comprising carbon and oxygen located on a surface of the doped semiconductor substrate;
an epi Si layer located on a portion of said doped semiconductor substrate;
a gate region located on said epi Si layer; and
a strained SiGe layer located on said doped semiconductor substrate adjacent to said epi Si layer and said gate region, said strained SiGe layer serving as a raised layer for source/drain diffusion regions.
- [c2] The semiconductor structure of Claim 1 wherein the doped semiconductor substrate comprises a silicon-on-insulator (SOI) layer of an SOI substrate.
- [c3] The semiconductor structure of Claim 2 wherein said SOI layer has a thickness from about 10 nm to about 120 nm.
- [c4] The semiconductor structure of Claim 1 wherein said doped semiconductor substrate comprises an n-type dopant.

- [c5] The semiconductor structure of Claim 1 wherein said doped semiconductor substrate comprises a p-type dopant.
- [c6] The semiconductor structure of Claim 1 wherein said gate region comprises a gate dielectric, a gate electrode overlaying the gate dielectric, and at least one spacer located on a sidewall of said gate electrode.
- [c7] A method of forming a semiconductor structure comprising the steps of:
forming a monolayer comprising oxygen and carbon on a surface of a doped semiconductor substrate;
forming an epi Si layer atop the doped semiconductor substrate;
forming at least one gate region on the epi Si layer;
etching exposed portions of the epi Si layer, not protected by the gate region, stopping on and exposing the doped semiconductor substrate using end point detection; and
forming a raised and strained SiGe layer on the exposed doped semiconductor substrate.
- [c8] The method of Claim 7 wherein said forming said monolayer comprises atomic layer deposition.
- [c9] The method of Claim 7 wherein said forming said mono-

layer comprises a chemical treatment process.

- [c10] The method of Claim 9 wherein said doped semiconductor substrate is subjected to a hydrogen termination processing step prior to forming said monolayer by said chemical treatment process.
- [c11] The method of Claim 10 wherein said hydrogen termination processing step comprises contacting the first semiconductor layer with dilute hydrofluoric acid.
- [c12] The method of Claim 9 wherein said chemical treatment process comprises contacting the doped semiconductor substrate with a solution comprising iodine and an alcohol.
- [c13] The method of Claim 12 wherein said solution comprising iodine and an alcohol contains from about 1×10^{-4} to about 1×10^{-3} M iodine in alcohol.
- [c14] The method of Claim 12 wherein said alcohol comprises methanol.
- [c15] The method of Claim 7 wherein said end point detection comprises analyzing effluents from a gas to detect at least one of carbon or oxygen in the monolayer.
- [c16] The method of Claim 7 wherein said end point detection comprises analyzing effluents from a gas to detect

dopants in said doped semiconductor substrate.

- [c17] The method of Claim 7 wherein said etching said epi Si layer comprises a selective etch process.
- [c18] The method of Claim 7 wherein said forming a raised and strained Si layer comprises growing an epitaxial SiGe film using conventional epitaxy reactors.
- [c19] The method of Claim 7 wherein said forming said at least one gate region comprises depositing a gate dielectric layer and a gate electrode material; patterning at least said gate electrode material; and forming at least one spacer on at least a sidewall of the patterned gate electrode.
- [c20] The method of Claim 7 wherein said forming said at least one gate region comprises a damascene process in which a dummy gate region is employed.